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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,690	07/20/2006	Tadatomo Suga	YANE-0003-US1	6233

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EXAMINER	
PATEL, DEVANG R	
ART UNIT	PAPER NUMBER
1793	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,690	SUGA ET AL.	
	Examiner	Art Unit	
	DEVANG PATEL	1793	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-50* is/are pending in the application.

4a) Of the above claim(s) *21 and 26-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-20,22-25,50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 2, 5, 13, 15, 17-19, and 22-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suga et al. (**WO 2002017378 A1**). US 2003/0164396 A1 is taken to be English-language equivalent of WO 2002017378 and sections pointed out in the rejection below refer to the US publication.

a. **Regarding claim 2,** Suga et al. (**"Suga"**) discloses a bonding method [¶ 9; fig. 1] for bonding objects to be bonded which have a bonding portions (2a) formed of a metal, wherein the bonding portions include gold/tin or gold/gold bonding [¶ 10], and such gold-gold bonding portions inherently have a hardness of 200 Hv or less. Suga discloses that before bonding, the bonding portions are treated with an energy wave such as plasma or ion beam or atomic beam [¶ 11]. Suga does not expressly disclose bonding at room temperature after treating, however, Suga does teach that energy wave irradiation of energy wave can be aimed to activate the surface up to a degree at which room-temperature bonding becomes possible [¶ 11]. Thus, one skilled in the art reading Suga would have understood and appreciated the possibility of room-temperature bonding due to energy wave treatment resulting in activated surfaces. In view of that, it would

have been obvious to a person of ordinary skill in the art at the time of the invention to carry out bonding at room temperature in the method of Suga because such avoids necessary heating for bonding and thus, saves associated energy and cost. Moreover, the claim would have been obvious because a person of ordinary skill has good reason to pursue the known options (focused energy wave treatment) within his or her technical grasp and if this leads to the anticipated success (room-temperature bonding), it is likely the product not of innovation but of ordinary skill and common sense.

b. **As to claim 5,** Suga discloses atmospheric-pressure (i.e. low-pressure) plasma [¶ 11].

c. **As to claim 13,** Suga discloses the bonding method, wherein in a chamber (7) having a reduced pressure, the bonding portions are treated with energy wave while bonding surfaces are not facing each other (in cleaning chamber 6), and thereafter, Suga discloses moving at least one of the objects (by conveying means 8 - ¶ 24-25) so that the bonding surfaces are contacted with each other in the chamber 7 [fig. 1].

d. **As to claim 15,** Suga discloses that the bonding portion is formed in the shape of a contour, said bonding portion is surface-activated with said energy wave, and thereafter, said objects to be bonded are bonded together in a solid phase at room temperature, so that space surrounded in said shape of contour by said bonding portions is formed between said bonding surfaces of said objects to be bonded to enclose a predetermined atmosphere in said space.

e. **As to claim 17,** Suga discloses that room-temperature bonding is performed in a vacuum [¶ 11].

f. **As to claim 18,** Suga discloses that after said surface activation of said bonding portion, a vacuum state of a low- pressure chamber is replaced with filling gas, and said objects to be bonded are bonded in said filling gas to enclose said filling gas atmosphere in said space [figs. 1, 4-5; ¶ 36-39].

g. **As to claim 19**, Suga discloses bonding in air [fig. 4].

h. **As to claim 22,** Suga discloses the objects to be bonded are a chip and a wafer (substrate) [¶ 1-2, 5]. It is well known in the art to continuously bond plurality of wafers at room-temperature after energy wave treatment [¶ 5]. The claim would have been obvious because continuously bonding plurality of chips to a wafer was recognized as part of ordinary capabilities of one skilled in the art and would have yielded the predictable result of forming desired semiconductor device.

i. **As to claims 24 & 25,** Suga discloses semiconductor device (IC chip 2).

3. **Claims 3-4 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suga et al. as applied to claim 2 above, and in view of Gilleo et al. (US 5971253, of record).

j. **As to claim 3,** Suga discloses gold/gold bonding, however, it is unclear whether Suga discloses forming a gold film on a surface of a base material (pads 14a) having a hardness of 200 Hv or less, and after bonding, the gold film is diffused into the base material. Gilleo et al. ("**Gilleo**") is drawn to microelectronic

component mounting. Gilleo discloses [fig. 3] copper pads 56 (analogous to pads 14a of Suga) on the substrate/chip 54, having a coating 58 (i.e. film) formed from gold or other diffusion bondable metal, and a diffusion bonding material 40 in conjunction with sheet 22 [figs. 8-9a; col. 7, lines 24-40]. The copper pads (base material) inherently have a hardness of 200 Hv or less. Diffusion bonding encompasses the gold film being diffused into the base material. Gilleo discloses that such bonding results in good connections even where the contacts of the chips and/or the pads of the substrate are slightly out of plane or of different heights [col. 7, lines 46-57]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the bonding technique of Gilleo in the method of Suga because doing so results in good connections even where the contacts of the chips and/or the pads of the substrate are slightly out of plane or of different heights.

k. **As to claim 4,** both Suga and Gilleo disclose the object being a semiconductor. Gilleo discloses diffusing a gold film into the copper base material as explained in claim 3 above.

l. **As to claim 14,** Suga and Gilleo as a whole discloses that bonding portion is treated with said energy wave, a metal electrode is provided at a position facing said bonding surface of at least one of said objects to be bonded, forming a metal film. Suga also discloses that sputtering the bonding surfaces in room-temperature bonding method of silicon wafers is known [¶ 5]. It would have been obvious to form the metal film by sputtering in the bonding method of Suga since

the technique of sputtering was recognized as part of ordinary capabilities of one skilled in the art.

4. **Claims 6, 8 and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suga et al. as applied to claims 5 and 22 above, respectively, and in view of Yamauchi (US 2004/0169020, of record).

m. **As to claim 6,** Suga does not expressly disclose generating plasma by an alternating power supply. However, **Yamauchi** (also drawn to room-temperature chip bonding after plasma treatment) discloses that low-pressure plasma for cleaning is generated with electric field having alternating + and - directions generated by an alternating power supply 11/25/150 [figs. 1-4, 16-18]. In view of that, it would have been obvious to a person of ordinary skill in the art at the time of the invention to employ alternating power supply of Yamauchi in the bonding method of Suga since such is art-recognized technique for plasma generation.

n. **As to claim 8,** in accordance with broadest reasonable interpretation, the oscillating power supply of Yamauchi in the method of Suga (as explained in claim 6 above) is equivalent to a wave generating power supply capable of controlling a pulse width.

o. **As to claim 23,** it is unclear whether Suga discloses that after a predetermined time has passed, the wafer is treated again with said energy wave. However, Yamauchi discloses that after predetermined time (in cleaning chamber), chips 2 and substrate 3 are conveyed and simultaneously treated again by energy wave immediately before bonding [¶ 147]. It would have been

obvious to a person of ordinary skill in the art at the time of the invention to treat the bonding surfaces again with the energy wave in the method of Suga in order to provide sufficient activated surfaces to allow room-temperature bonding.

5. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Suga et al. in view of Yamauchi as applied to claim 6 above, and further in view of Linn et al. (US 5833758, of record).

p. **As to claim 7,** it is unclear whether Suga or Yamauchi discloses RF plasma generating power supply. However, Linn et al. (**"Linn"**, drawn to method for cleaning semiconductor wafers) discloses two-step RF plasma cleaning process for wafers [col. 4, line 66 thru col. 3, line 10]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide RF plasma generation similar to Linn in the method of Suga in order remove all contaminants from the surface and consequently improve bonding (Linn-abstract).

6. **Claims 9-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suga et al. as applied to claim 2 above, and in view of Linn et al. (US 5833758) and Usui et al. (US 2004/0140551).

q. **As to claim 9**, Suga fails to disclose the bonding portion having a surface roughness. However, **Linn** discloses that argon plasma cleaning (similar to Suga) roughens the surface and enhances the solderability to the substrate by increasing the surface of the bonding layer [col. 3, lines 12-15]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to

provide RF plasma generation similar to Linn in the method of Suga in order remove all contaminants from the surface and consequently improve bonding (Linn- abstract). Linn is silent about surface roughness value. However, Usui et al. (**"Usui",** drawn to manufacturing semiconductor device) discloses surface processing a metal film to form a patterned interconnect line and to achieve surface roughness of 1 micron or less (i.e. greater than 120 nm), which effectively improves the high frequency performance [¶ 24; claim 14]. The collective disclosures of Suga, Linn and Usui teaches a bonding portion having the surface roughness value 120 nm or more, and providing so would have been obvious to a person of ordinary skill in the art at the time of the invention in order to increase the surface area and improve bonding strength (Linn) and device performance (Usui).

r. **As to claim 10,** Suga discloses the bonding method including:

i. a head 16 [fig. 1] for holding one of the objects to be bonded;

ii. a stage 15 for holding the other object to be bonded; and

iii. a vertical drive mechanism for performing a position control with respect to at least one of said head and said stage in a direction substantially perpendicular to said bonding surface of said object to be bonded, and performing a pressing control [¶ 26],

iv. the vertical drive mechanism of Suga is implicitly stopped at some point, when the bumps 2a and pads 14a are being bonded, thus it holds a constant height of the head 16 from said stage for a predetermined time.

7. **Claims 11-12 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suga as applied to claims 1 and 19 above, respectively, and in view of Yagi et al. (US 5686353).

s. **As to claim 11-12,** Suga does not disclose leveling the bonding portion. However, such is well known in the art. Yagi et al. ("**Yagi**") discloses leveling step to obtain uniform height of each of the bumps, and adapting the height of each of the bumps to corresponding height of each of the electrodes on the substrate [col. 5, line 33 thru col. 6, line 20]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to perform leveling similar to Yagi in the method of Suga in order to avoid the difficulties of non-uniformity and insufficient bonding strength [col. 3, lines 6-11].

t. **As to claim 20,** Suga discloses electrically functioning device that employs the bonding portion as an electrode, bonding portion formed of gold, and cleaned with energy wave before bonding in air. However, it is unclear whether Suga discloses adjusting optimum positions of the objects to be bonded while the device is caused to electrically function. **Yagi** discloses positioning the semiconductor device (i.e. chip) in relation to the substrate in a manner so as to transform the apex portion of each of the bumps and thus adapt height of each of the bumps to each of corresponding electrodes [col. 6, lines 4-12]. Yagi further states that such provides extreme stability and accuracy, even if the electrodes have irregularity of thickness, or if the substrate has a warp. Yagi also discloses that the function test the electrical circuit is performed when the device is pressed

against the substrate [col. 6, lines 22-28]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to perform positioning step of Yagi in the method of Suga because it provides extreme stability and accuracy, even if the electrodes have irregularity of thickness, or if the substrate has a warp or undulation [col. 6, lines 13-21].

8. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Suga as applied to claim 15 above, and in view of Usui et al. (US 5686353).

u. **As to claim 16,** Suga discloses bonding portion formed of gold but does not disclose the base material having hardness of 200 Hv or less, and a gold plating having a thickness of 1 micron or more. However, such arrangement is well known in the art as shown by Usui. **Usui** (directed to semiconductor device mounting) discloses a gold film 402 having a thickness of about 1-10 micron on a copper base material 400 [fig. 5a; ¶ 79]. The copper base material inherently has a hardness of 200 Hv or less. It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide the copper base and gold plating similar to Usui in the method of Suga because doing so results in better adhesiveness and better plating [¶ 79], thus improving bonding strength.

9. **Claim 50** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi (**WO 2003001858 A1**) in view of applicant admitted prior art (referring as **AAPA -** JP 2791429 B). US 2004/0169020 is taken to be English-language equivalent

of WO 2003001858 A1 and sections pointed out in the rejection below refer to the US publication.

v. **Regarding claim 50, Yamauchi** discloses a bonding method [fig. 1; ¶ 8-11] for bonding objects to be bonded which have a bonding portion (4, 5) formed of a metal, wherein the bonding portions are gold/gold bonding, which inherently have a hardness of 200 Hv or less. The bonding portions are contacted with each other and pressed in a solid phase at low temperature of about 150 ºC after treating the bonding portions with plasma [¶ 142-143].

w. Yamauchi discloses bonding in a vacuum condition [¶ 28] but does not disclose low vacuum of 10^{-5} torr or more. However, **AAPA** discloses that it is known to perform surface activating treatment and subsequent bonding in a high vacuum of 10^{-5} torr or more [¶ 13 of publication]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to carry out bonding at claimed vacuum range in the method of Yamauchi since such is well-known in the art. Moreover, it would have been obvious to one of ordinary skill in the art at the time of the invention to choose the instantly claimed ranges through process optimization, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. Thus, in the method of Yamauchi and AAPA, under vacuum of about 10^{-5} torr, adhering substance layer would intrinsically form on the bonding surfaces, and consequently crushed at the time of bonding.

10. **Claim 50** is rejected under 35 U.S.C. 103(a) as being unpatentable over Suga et al. (**WO 2002017378 A1**) in view of **AAPA** (JP 2791429 B). US 2003/0164396 A1 is taken to be English-language equivalent of WO 2002017378 and sections pointed out in the rejection below refer to the US publication.

x. **Regarding claim 50, Suga** discloses a bonding method [¶ 9; fig. 1] for bonding objects to be bonded which have a bonding portions (2a) formed of a metal, wherein the bonding portions include gold/tin or gold/gold bonding [¶ 10], and such gold-gold bonding portions inherently have a hardness of 200 Hv or less. Suga discloses that before bonding, the bonding portions are treated with an energy wave such as plasma or ion beam or atomic beam [¶ 11]. Suga does not expressly disclose bonding at room temperature after treating, however, Suga does teach that energy wave irradiation of energy wave can be aimed to activate the surface up to a degree at which room-temperature bonding becomes possible [¶ 11]. Thus, one skilled in the art reading Suga would have understood and appreciated the possibility of room-temperature bonding due to energy wave treatment resulting in activated surfaces. In view of that, it would have been obvious to a person of ordinary skill in the art at the time of the invention to carry out bonding at room temperature in the method of Suga because such avoids necessary heating for bonding and thus, saves associated energy and cost. Moreover, the claim would have been obvious because a person of ordinary skill has good reason to pursue the known options (focused energy wave treatment) within his or her technical grasp and if this leads to the anticipated success

(room-temperature bonding), it is likely the product not of innovation but of ordinary skill and common sense.

y. Suga discloses bonding in a vacuum condition [¶ 11] but does not disclose low vacuum of 10^{-5} torr or more. However, **AAPA** discloses that it is known to perform surface activating treatment and subsequent bonding in a high vacuum of 10^{-5} torr or more [¶ 13 of publication]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to carry out bonding at claimed vacuum range in the method of Suga since such is well-known in the art. Moreover, it would have been obvious to one of ordinary skill in the art at the time of the invention to choose the instantly claimed ranges through process optimization, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. Thus, in the method of Suga and AAPA, under vacuum of about 10^{-5} torr, adhering substance layer would intrinsically form on the bonding surfaces, and consequently crushed at the time of bonding.

Response to Amendment and Arguments

Applicant's arguments, filed 4/6/09, with respect to the rejection(s) of amended claim(s) 2-20, 22-25 and 50 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Suga et al. (WO 2002017378 A1) and so applicant's arguments are moot in view of the new ground(s) of rejection set forth above.

Conclusion

Claims 2-20, 22-25 and 50 are rejected.

The rejections above rely on the references for all the teachings expressed in the text of the references and/or one of ordinary skill in the art would have reasonably understood from the texts. Only specific portions of the texts have been pointed out to emphasize certain aspects of the prior art, however, each reference as a whole should be reviewed in responding to the rejection, since other sections of the same reference and/or various combinations of the cited references may be relied on in future rejections in view of amendments.

Applicant is reminded to specifically point out the support for any amendments made to the disclosure. See 37 C.F.R. 1.121; 37 C.F.R. Part 41.37; and MPEP 714.02.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVANG PATEL whose telephone number is (571)270-3636. The examiner can normally be reached on Monday thru Thursday, 8:00 am to 5:30 pm, EST..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jessica Ward can be reached on 571-272-1223. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. P./
Examiner, Art Unit 1793

/Kuang Y. Lin/

Primary Examiner, Art Unit 1793